AMENDMENTS TO THE SPECIFICATION

The paragraph commencing at page 2, line 21 is amended as follows:

As shown in Fig. 8, the current-mirror band gap circuit has a p-type transistor ~~P1~~ P11, a p-type transistor ~~P2~~ P12, an n-type transistor ~~N1~~ N11, and an n-type transistor ~~N2~~ N12. A p-type transistor ~~P3 is~~ P13 has its gate connected between the n-type transistor ~~N2~~ N12 and the p-type transistor ~~P2~~ P12 in this current-mirror band gap circuit.

The paragraph commencing at page 3, line 2 is amended as follows:

Furthermore, as shown in Fig. 8, in this current-mirror band gap circuit, a resistor ~~R1~~ R11 and a diode ~~D2~~ D12 are connected between the n-type transistor ~~N2~~ N12 and a negative power supply point. And, a resistor ~~R2~~ R12 and a diode ~~D3~~ D13 are connected between an output terminal VOUT and the negative power supply. Furthermore, the diode ~~D1~~ D11 is connected between the n-type transistor ~~N1~~ N11 and the negative power supply. Also, these resistors ~~R1~~ R11 and ~~R2~~ R12, and diodes ~~D2~~ D12 and ~~D3~~ D13 have a function of discharging a current that transitionally flows into the output terminal VOUT at the time of introducing the power supply and of fluctuation thereof.

The paragraph commencing at page 3, line 24 is amended as follows:

Fig. 10 illustrates the conventional differential band gap circuit. As shown in Fig. 10, the differential band gap circuit has a differential amplifier to be configured of a pair of p-type transistors P1 and P2, and a pair of n-type transistors N1 and N2. This differential amplifier has the p-type transistor P3 connected between the p-type transistor P2 and the n-type transistor N2 thereof, and this p-type transistor P3 is connected to the output terminal VOUT.

The paragraph commencing at page 4, line 8 is amended as follows:

The resistor R2, and the resistor R1 and the diode D1, which are connected between this

resistor R2 and the ground, are connected to the output terminal VOUT in this order. Also, as shown in Fig. 10, in addition to these resistors R1 and ~~R2,~~ R2 and the diode D1, the resistor ~~R2~~ R3 and the diode D2 are connected between the output terminal VOUT and the ground in this order. A noninverting terminal of the differential amplifier is connected between the resistor R1 and the resistor R2, and an inverting terminal thereof is connected between the resistor ~~R2~~ R3 and the diode D2. Also, in the differential band gap circuit, similarly to the current-mirror band gap circuit, the current, which flows into the output terminal VOUT, is discharged from the resistors R1, R2, and ~~R2~~ R3, and the diodes D1 and D2. ~~to be connected to the output terminal VOUT.~~

The paragraph commencing at page 9, line 20 is amended as follows:

The band gap circuit relating to the present invention that is a band gap circuit for generating an output voltage to output it from a circuit output terminal, which is connected to a power supply voltage and a reference potential, said band gap circuit comprises: a differential amplifier (for example, a differential amplifier to be configured of n-channel transistors N4 and N5, and p-channel transistors P6 and P7 in the embodiments of the present invention) having an inverting input terminal, a noninverting input terminal, and an output terminal; a first circuit (for example, a circuit to be configured of resistors R1, R2, and ~~R2~~ R3, and diodes D1 and D2 in the embodiments of the present invention) for causing a potential difference to occur at said inverting input terminal and said noninverting input terminal responding to fluctuation of the voltage of said circuit output terminal; a switching element (for example, an n-channel transistor N3 in the embodiments of the present invention) for causing an excess current of said circuit output terminal to flow in said reference potential responding to fluctuation of the potential at said output terminal of said differential amplifier, said switching element being connected to said circuit output terminal, said reference potential, and said output terminal of said differential amplifier; a first element

(for example, a p-channel transistor P5 in the embodiments of the present invention) having a resistive component, said first element being connected to said power supply voltage and said circuit output terminal; and a second element (for example, a ~~resistor~~ resistors R2 and R3 in the embodiments of the present invention) having a capacitive component, said second element being connected to the above first element. Such a configuration allows the current noise of the power supply voltage to be removed, and the excess current, which transitionally sneaks into the circuit output terminal, to be removed surely and efficiently.

The paragraph commencing at page 15, line 8 is amended as follows:

The drain of the p-type transistor P6 is connected to the drain of the n-type transistor N4, and the source thereof is connected to the power supply voltage VDD via a p-type transistor P14. Also, as shown in Fig. 1, the gate of the p-type transistor P6 is connected to the output terminal VOUT via the resistor R2. As to the p-type transistor P7, similarly to the p-type transistor P6, its drain is connected to the drain of the n-type transistor N5, and its source is connected to the power supply voltage VDD via the p-type transistor P14. Also, as shown in Fig. 1, the gate of the p-type transistor P7 is connected to the output terminal VOUT via the resister ~~R2~~ R3. Resistors R2 and R3 have substantially the same resistance value.

The paragraph commencing at page 15, line 20 is amended as follows:

As shown in Fig. 1, the resistor R2, the ~~register~~ resistor R1, and the diode D1 are connected between the output terminal VOUT and the ground in the order of their being located on the output terminal VOUT side. In addition hereto, the resistor ~~R2~~ R3 and the diode D2 are connected between the output terminal VOUT and the ground in the order of their being located on the output terminal VOUT side.

The paragraph commencing at page 16, line 10 is amended as follows:

The cathode of the diode D2 is earthed to the ground, and its anode is connected to the resistor ~~R2~~ R3 and the gate of the p-type transistor P7. The resistor R2 has one end thereof connected to the resistor R1 and the gate of the p-type transistor P6, and the other connected to the output terminal VOUT.

The paragraph commencing at page 16, line 16 is amended as follows:

The resistors R1, R2, and ~~R2~~ R3, and diodes D1 and D2 are connected between the output terminal VOUT and the ground in such a manner, and the gate of the p-type transistor P6 functions as the noninverting input terminal of the differential amplifier. Together therewith, the gate of the p-type transistor P7 functions as the inverting input terminal of the differential amplifier. The differential amplifier, as a rule, performs the operation so that the noninverting input terminal and the inverting input terminal have the almost identical potential. This operation is utilized to cause the potential of the anode of the diode D2 and the potential of the resister R1 on the power supply side to become equal for generating the constant current.

The paragraph commencing at page 17, line 5 is amended as follows:

Also, the ~~resistor~~ resistors R1, R 2 and ~~the resistor R2~~ R3 are not limited to the general resistive element, but also can be formed, for example, by employing ~~the~~ an element having ~~the~~ a resistive component, such as ~~the~~ a transistor. Also, the ~~resister~~ resistors R1, ~~and the resistor~~ R2, and R3 should be an N well resistor formed on a substrate such as a silicon substrate. Herein, the so-called N well resistor is a diffused resistor wherein the parasitic capacity sticks between the substrate and an N well. Also, the so-called N well resistor is an ion implantation resistor having the N well formed, for example, by means of an ion implantation method. In the event of employing the N well resistor to form the resistors R1, ~~and~~ R2 and R3, they can be formed simultaneously in forming the other transistor, whereby

the resistor can be formed easily.

The paragraph commencing at page 21, line 21 is amended as follows:

As shown in Fig. 1, the gate of p-type transistor P14 is connected to the constant voltage source 20 and the gate of p-type transistor P4. The p-type transistor P14 has the drain thereof connected to the differential amplifier, and the source connected to the power supply voltage VDD. And, the gate of p-type transistor P14 is supplied with the bias voltage Vb1 from the constant voltage source 20. The p-type transistor P14 supplies the current from the power supply voltage VDD to the differential amplifier responding hereto. Also, as shown in Fig. 1, a p-type transistor P24 within the constant voltage source 20 to be described later, the p-type transistor P4, and the p-type transistor P14 configure the current mirror circuit. Additionally, in Fig. 1, the p-type transistor P14 is connected to the differential amplifier.

The paragraph commencing at page 22, line 10 is deleted.

The paragraph commencing at page 31, line 7 is amended as follows:

When the voltage of the output terminal VOUT rises, the sneak current is discharged at the resistors R1, R2, and ~~R2~~ R3, and the diodes D1 and D2. As shown in Fig. 5A, when the sneak current is discharged by the resistors R1, R2, and ~~R2~~ R3, and the diodes D1 and D2 etc. and is reduced, the voltage of the output terminal VOUT lowers and then is stabilized. Together therewith, as shown in Fig. 5B, the drain current of the p-type transistor P3 lowers and then is stabilized.

The paragraph commencing at page 35, line 9 is amended as follows:

The p-type transistor P5 has the drain thereof connected to the output terminal VOUT, and the source connected to the drain of the p-type transistor P4. The drain of the p-type transistor P4 was connected to the output terminal VOUT in the band gap circuit in the embodiment 1; however it is connected to the source of the p-type transistor P5 in the band gap circuit of the embodiment 2. Furthermore, as shown in Fig. 2, the p-type transistor P5 is connected to the output terminal VOUT, and is connected to the ~~resistor~~ resistors R2 and R3 via the output terminal VOUT.

The paragraph commencing at page 36, line 6 is amended as follows:

The constant voltage source 20a, to which the gate of the p-type transistor P5 is connected, is configured similarly to that of the embodiment 1. The constant voltage source 20a of the embodiment 2 has a constant current source 21, a p-type transistor P24, and further has a p-type transistor P25 to be connected to the p-type transistor P5. The p-type transistor P25 has the drain thereof connected to the constant current source 21, and the source connected to the drain of the p-type transistor P24. The drain of the p-type transistor P24 was connected to the ~~direct-current power supply~~ constant current source 21 in the band gap circuit of the embodiment 1; however it is connected to the source of the p-type transistor P25 in the band gap circuit of the embodiment 2. Also, the p-type transistor P25 has the connection (diode connection) made between the drain and the gate thereof similarly to the p-type transistor P24.

The paragraph commencing at page 36, line 23 is amended as follows:

The gate of the p-type transistor P25 is supplied with the bias voltage Vb2 from the

constant voltage source 20a, and is connected to the gate of the p-type transistor P5. Together therewith, the gate of the p-type transistor P25 is connected to the gate of the p-type transistor P15. And, the gate of the p-type transistor P24 is supplied with the bias voltage ~~Vb2~~ Vb1 from the constant voltage source 20a, and is connected to ~~both~~ the gates of both the p-type transistors P4 and P14. Additionally, the p-type transistor P24 of the constant voltage source 20a is connected to the p-type transistors P14 and P4 to configure the current mirror circuit. Also, the p-type transistor P25 of the constant voltage source 20a is connected to the p-type transistors P15 and P5 to configure the current mirror circuit.

The paragraph commencing at page 38, line 10 is amended as follows:

In the band gap circuit of the embodiment 2, as shown in Fig. 2, the p-type transistor P5, and the ~~resistor~~ resistors R2 and R3 on the output terminal VOUT side are connected via the output terminal VOUT. This allows the p-type transistor P5, and the ~~resistor~~ resistors R2 and R3 on the output terminal VOUT side to function as a low-pass filter. The low-pass filter is configured of the p-type transistor P5 having the resistive component, and the ~~resistor~~ resistors R2 and R3 having the capacitive component. Resistors R2 and R3 have substantially the same resistance value.

The paragraph commencing at page 38, line 19 is amended as follows:

For example, in the band gap circuit of the embodiment 2, the p-type transistor P5 is capable of functioning as a resistive element having the resistive component that corresponded to a decline in the voltage between the source and the drain of the p-type transistor P5. Also, in the event that the ~~resistor~~ resistors R2 and R3 on the output terminal

VOUT side ~~is an~~ are N well ~~resistor~~ resistors formed on the substrate such as the p-type silicon substrate, the ~~resistor~~ resistors R2 and R3 ~~functions~~ function as a capacitive element having the capacitive component that corresponded to the parasitic capacity that sticks between the substrate and the N well.

The paragraph commencing at page 39, line 5 is amended as follows:

Herein, the so-called N well resistor is a diffused resistor wherein the parasitic capacity sticks between the substrate and the N well, and also is an ion implantation resistor having the N well formed, for example, by means of the ion implantation method. For this, by employing the N well formed by means of the ion implantation method etc. as the ~~resistor~~ resistors R2 and R3 on the output terminal VOUT side, the low-pass filter can be configured. In the event of employing the N well resistor to form the ~~resistor~~ resistors R2 and R3 in such a manner, it can be formed simultaneously in forming the other transistor, and the resistor having the capacitive component can be formed easily.

The paragraph commencing at page 39, line 17 is amended as follows:

Also, as a rule, when a gate length of the p-type transistor P5 is lengthened, as shown in Fig. 3, the current characteristic of the source-drain can be stabilized, and the situation can be extended in which the current is kept constant against the voltage. And, by lengthening the gate length of the p-type transistor P5, it can be employed as a resistive element having the resistive component. For this, in the event of configuring the low-pass filter of the p-type transistor P5 and the ~~resistor~~ resistors R2 and R3 on the output terminal VOUT side, the gate length of the p-type transistor P5 is desirably lengthened. As one example, the gate length of the p-type transistor P5 is preferably taken as 2μm or more.

The paragraph commencing at page 40, line 5 is amended as follows:

In such a manner, by employing the N well resistor for the ~~resistor~~ resistors R2 and R3 on the output terminal VOUT side, the parasitic capacity can be positively utilized to configure the low-pass filter that removes the noise having the frequency higher than a certain level. This allows the power supply noise of the high-frequency region to be included in the current from the power supply voltage VDD to be surely removed in the band gap circuit of the embodiment 2.

The paragraph commencing at page 41, line 2 is amended as follows:

Also, additionally, the ~~resistor~~ resistors R2 and R3 on the output terminal VOUT side ~~was~~ were taken as ~~the~~ N well ~~resistor~~ resistors for configuring the low-pass filter in the band gap circuit of the embodiment 2; however it is not limited to this, and the element having the parasitic resistance and the element having the capacitive component such as the capacity are acceptable. Or, the element having the capacitive component may be provided between the output terminal VOUT and the ~~resistor~~ resistors R2 and R3 on the output terminal VOUT side in addition to the ~~resistor~~ resistors R2 and R3. Also, or, the low-pass filter may be configured by taking the ~~resistor~~ resistors R2 and R3 on the p-type transistor P5 side as the N well resistor. By employing the ~~resistor~~ resistors R2 and R3 having the parasitic resistance as the element having the capacitive component like it is employed in the band gap circuit of the embodiment 1, the element having the capacitive component can be formed easily and efficiently. Furthermore, by employing the ~~resistor~~ resistors R2 and R3 having the parasitic resistance for both of the resistors R2 and R3 on the output terminal VOUT side and on the p-type transistor P5 side, the function as the low-pass filter can be enhanced.

The paragraph commencing at page 45, line 2 is amended as follows:

Furthermore, in the band gap circuit of the embodiment 2, the low-pass filter for removing the power supply noise in the high-frequency region of the power supply voltage VDD is configured of the p-type transistor P5 and the ~~resistor~~ resistors R2 and R3 of the output terminal VOUT. For this, differently from the PSRR of the conventional band gap circuit, and the band gap circuit of the embodiment 1, at the moment that the PSRR is stabilized after it lowered, the PSRR in the band gap circuit of the embodiment 2 gently rises. The PSRR after stabilization becomes 20 dB to 30 dB or something like this because the PSRR in the band gap circuit of the embodiment 2 is constantly kept at a higher value than that of the conventional band gap circuit, which is a higher value than that of the conventional band gap circuit.

The paragraph commencing at page 46, line 5 is amended as follows:

As shown in Fig. 4, in the band gap circuit of the embodiment 2, differently from the band gap circuit of the embodiment 1, the n-type transistor N3 is connected to the differential amplifier, and the p-type transistor P5 is connected to the output terminal VOUT. The low-pass filter to be connected to the power supply voltage VDD is configured of this p-type transistor P5 and ~~resistor~~ resistors R2 and R3 on the output terminal VOUT side, thus allowing the current noise, which is apt to occur in the high-frequency region, to be surely removed. For this, it becomes possible that the PSRR is raised in the high-frequency region for stabilizing it at a higher value than that of the case of the embodiment 1.

The paragraph commencing at page 47, line 20 is amended as follows:

When the voltage of the output terminal VOUT rises, the sneak current is discharged at the resistors R1, R2, and ~~R2~~ R3, and the diodes D1 and D2. Also, as shown in Fig. 5B, the sneak current flows into the p-type transistor P3 as well, thus causing the drain current to rise further from the rising level caused by the introduction of the power supply. Thereafter, as shown in Fig. 5A, when the sneak current is discharged by the resistors R1, R2, and ~~R2~~ R3, and the diodes D1 and D2 etc. and is reduced, the voltage of the output terminal VOUT lowers and then is stabilized. Together therewith, as shown in Fig. 5B, the drain current of the p-type transistor P3 lowers and then is stabilized.

The paragraph commencing at page 49, line 4 is amended as follows:

Furthermore, in the band gap circuit of the embodiment 2, the p-type transistor P5 is connected to the output terminal VOUT to configure the low-pass filter together with the ~~resistor~~ resistors R2 and R3 on the output terminal VOUT side. For this, the power supply noise is removed in the high-frequency region of the power supply voltage VDD with the low-pass filter in supplying the current to the output terminal VOUT.